

Errata and Cautions

Microprocessor access of sample memory

The 1K addresses sample memory by adding 3 numbers: the address specified by the instruction, the sample downcounter, and (in some instructions) a masked data dependent number.

The address of sample memory for external access is determined solely by the address written to the 1K.

In order for the address of sample memory to agree between external

access and the 1K's internal access, the value in the downcounter must be zero. This can be achieved by never allowing the value of Control Word 1 bits 1 and 0 to be any value other than 1 and 0, respectively.

If the value of those bits ever changes (after reset) the downcounter runs and (for all practical purposes) the value of the downcounter cannot be known outside the 1K.

Serial access of sample memory

Whenever the 1K's memory is externally accessed, enough time must be allowed for the access to complete before any changes are made to the mechanisms that control the memory access. In the case of external serial writes to sample memory using the "sample 1023" method, this means that there must be no transitions on the CLOCK (D1) pin after the last data bit is clocked in until the start of the next sample period. If the WORDCLK is not being monitored to determine when the next sample period begins, then a one-sample-period delay should be incorporated after the last data bit. This is 21 microseconds for a 48 kHz WORDCLK.

For example, when sending word after word using the address-autoincrement feature, a wait of 21 microseconds must be included between the last bit of one word and the first bit of the next. Likewise, after the last word is sent, there must be a 21 microsecond

delay before sending a deselect sequence (because the deselect sequence includes a clock transition).