Errata and Cautions

Microprocessor Access of Data RAM

The DSP-1K addresses Data RAM by adding 3 numbers: the address specified by the instruction, the Memory Control Unit's down counter, and (in some instructions) a masked data dependent number.

The address of Data RAM for external access is determined solely by the address written to the DSP-1K.

In order for the address of Data RAM to agree between external microprocessor access and the DSP-1K's internal program access, the value in the down counter must be zero. This may be achieved by never allowing the value of Control Word 1 bits 1 and 0 to be any value other than 1 and 0, respectively.

If the value of those bits ever changes after reset, the down counter will start running, and for all practical purposes the value of the down counter cannot be known outside the DSP-1K.

Serial Access of Data RAM

Whenever the DSP-1K's memory is externally accessed, enough time must be allowed for the access to complete before any changes are made to the mechanisms that control the memory access. In the case of external serial microprocessor writes to Data RAM using the Last Data Access Function, this means that there must be no transitions on the CLOCK (D1) pin after the last data bit is clocked in until the start of the next sample period. If the WORDCLK is not being monitored to determine when the next sample period begins, then a one-sample-period delay should be incorporated after the last data bit, which is 21 microseconds for a 48kHz WORDCLK.

For example, when sending sequential instructions words using the address-autoincrement feature, a wait of 21 microseconds must be included between the last bit of one word and the first bit of the next. Likewise, after the last word is sent, there must be a 21 microsecond delay before sending a deselect sequence (because the deselect sequence includes a clock transition).

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Application note revised December, 2005